

associative array processor pdf

PDF | Associative Processor (AP) combines data storage and data processing, and functions simultaneously as a massively parallel array SIMD processor and memory. Traditionally, AP is based on CMOS ...

(PDF) Resistive Associative Processor - ResearchGate

A production implementation of an associative array processor-ST ARAN by JACK A. RUDOLPH Goodyear Aerospace Corporation Akron, Ohio INTRODUCTION

A production implementation of an associative array

An associative array processor is described wherein an array (ARRAY) of associative processing cells is configured according to a format defined by configuration bits which perform functions previously performed by external masks.

EP0121763A2 - Associative array processor - Google Patents

pattern-processing applications is discussed last. ORGANIZATION AND COMMAND SET The addition operation presented in the preceding section is a typical example of the associative processing technique. From it, several conclusions concerning the desired structure for an associative processor can be formulated. 1.

AN ASSOCIATIVE PARALLEL PROCESSOR WITH APPLICATION TO

An Associative Processor Array Designed for Computer Vision ... of associative processors in a taxonomy of processors is explained and the innovations that have been made to the associative processor array concept are outlined. The most effective use of processor arrays requires

An Associative Processor Array Designed for Computer Vision

Associative Processor Architecture--A Survey S.S. YAU and H.S. FUNG ... Associative Linear Array Processor (ALAP) ECAM Other Developments ... associative processors belong to the general category called SIMD (Single Instruction Stream Multiple Data Stream) machines [5, 24]. ...

Associative Processor Architecture--A Survey S.S. YAU

Abstract--" Associative Processor (AP) combines data storage and data processing, and functions simultaneously as a massively parallel array SIMD processor and memory. Traditionally, AP is based on CMOS technology, similar to other classes of massively parallel SIMD processors. The main component of AP is a Content Addressable Memory (CAM) array.

L. Yavits, S. Kvatinsky, A. Morad, and R. Ginosar

Since the Associative Processing Array is byte-serial, the Control Unit must loop to process any field that is longer Figure 2 --" ASC Processor (Small Initial Prototype)

Implementing Associative Processing: Rethinking Earlier

This paper defines a high-level programming language for a generalized associative array processor (AP). In particular, a data management language for APs, known as DMAP, is developed for use with a representative AP model.

DMAP-a COBOL extension for associative array processors

SPARSE MATRIX MULTIPLICATION ON AN ASSOCIATIVE PROCESSOR L. Yavits, A. Morad, R. Ginosar

Abstractâ€”Sparse matrix multiplication is an important component of linear algebra computations. Implementing sparse matrix multiplication on an associative processor (AP) enables high level of parallelism, where a row of one matrix is multiplied in

SPARSE MATRIX MULTIPLICATION ON AN ASSOCIATIVE PROCESSOR

The associative or content-addressed memory has been an attractive concept to computer designers ever since Slade and McMahon's 1957 paper described a "catalog" memory.

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