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Verification by Error Modeling: Using Testing Techniques

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Verification by error modeling : using testing techniques

After the polynomial is converted to AT, its exact implementation can be verified using equivalence checking, while an imprecise one is checked through the search for maximal imprecision.

Verification by error modeling: using testing techniques

1. DESIGN FLOW Integrated circuit (IC) complexity is steadily increasing. ICs incorporating hundreds of millions of transistors, mega-bit memories, complicated pipelined structures, etc., are now in high demand.

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A design verification methodology for microprocessor hardware based on modeling design errors and generating simulation vectors for the modeled errors via physical fault testing techniques is presented.

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Model Verification and Validation

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14 Model Validation and Veriï-•cation 14.1 Introduction Whatever modelling paradigm or solution technique is being used, the performance mea-sures extracted from a model will only have some bearing on the real system represented

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Formal Modeling and Verification of Time-Constrained ARQ Protocols with Event-B Rajaa Filali#1, Mohamed Bouhdadi#2 # LMPHE Laboratory University of Mohammed V, Faculty of sciences 4 Street Ibn Batouta, PB 1014 RP, Rabat, MOROCCO

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Verification and validation of computer simulation models is conducted during the development of a simulation model with the ultimate goal of producing an accurate and credible model. [1] [2] "Simulation models are increasingly being used to solve problems and to aid in decision-making.

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